



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,793	12/24/2003	Katsuto Tanahashi	032206	9788
38834 7590 08/10/2007 WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			EXAMINER MONDT, JOHANNES P	
			ART UNIT 3663	PAPER NUMBER
			MAIL DATE 08/10/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/743,793

Applicant(s)

TANAHASHI ET AL.

Examiner

Johannes P. Mondt

Art Unit

3663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,4-14 and 19-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-14 and 19-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____   | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Response to Amendment*

Amendment filed 5/7/07 forms the basis for this office action. In said Amendment applicants substantially amended the claim language by adding new claims 19-28.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1, 4-6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al (US 2003/0159644 A1) in view of prior art as admitted by Applicants ("APAA"). Yonehara et al teach a semiconductor substrate 1 ([0075] and [0113]) comprising a front face and a rear face that are both mirror-polished ([0095]), wherein said semiconductor substrate contains boron at a concentration in the range  $1 \times 10^{17} - 10^{20} \text{ cm}^{-3}$  (see [0149]) which range overlaps the claimed range in the sub-range  $10^{17} - 2 \times 10^{17} \text{ cm}^{-3}$ . In this regard it is noted that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Yonehara also teach that a crystal layer 10 is provided on the front face ([0150]), and that a minimum value of the concentration of boron, [B] (in atoms/ cm<sup>3</sup>) is defined for a required thickness, "t" (in μm), said required thickness being  $t=100\text{ nm}=0.1\text{ }\mu\text{m}$  (see [0150]) of the crystal layer that satisfies the inequality as claimed, i.e., said minimum concentration being  $[B]=10^{17}\text{ cm}^{-3}$  (see [0149]), because  $\exp(0.21 \times 0.1) \cong 1.021 \leq 10^{17} / [(2.2 \pm 0.2) 10^{16}] \cong R$ , wherein  $4.17 \leq R \leq 5$  within 1% accuracy, hence falls in the claimed relation for said required thickness and within the range of boron concentration (*N.B.: please note that an upper portion of the crystalline layer 3 is porous and hence is (1) another layer and (2) not truly crystalline when taken as a whole, because the porosity destroys the translational symmetry along the lattice vectors which is a defining property of crystallinity*). Yonehara et al do not necessarily teach the limitation that said semiconductor substrate meets a criterion of "an SFQR value  $\leq 70$  nm as a flatness of the front face". However, as admitted by Applicants as many as 40% of all conventionally produced wafers satisfy said criterion and therefore, by rule of statistics all one of ordinary skills in the art has to do is make enough of said wafers in order to be certain to have one that satisfies said criterion.

With regard to claim 14, in addition Yonehara et al teach a semiconductor element formed on the front face of said semiconductor substrate (solar battery: see Figures 16 and [0072]).

On claim 4: a maximum value of a thickness of the crystal layer 10 is defined by Yonehara to be  $20\text{ }\mu\text{m}$  (see [0150]), which does satisfy the claimed inequality for a required concentration of boron [B] (in atoms/cm<sup>3</sup>), said concentration being required to

be in the interval  $10^{17} - 10^{20} \text{ cm}^{-3}$  (see [0149]), hence  $10^{20}$  being one of all required values, because  $\exp(0.21 \times 20) = \exp(4.2) \cong 66.7 \leq 4166 \leq 10^{20} / (2.2 \pm 0.2) \times 10^{16} \leq 10^{20} / (2.2 \pm 0.2) \times 10^{16}$ .

*On claim 5:* the crystal layer 10 is a silicon crystal layer ([0078]) formed by epitaxial growth ([0149]).

*On claim 6:* the crystal layer is a silicon-germanium alloy crystal layer ([0078]).

3. **Claims 7-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara and APAA as applied to claim 2 above, and further in view of Fitzgerald (US 2002/0123167 A1). As detailed claim 2 is unpatentable over Yonehara et al in view of APAA. Neither necessarily teach the claimed layered structure of SiGe and Si. However, (a) there is a specific suggestion by Yonehara et al that a layered structure of SiGe on silicon could be used to generate stress in an SOI structure ([0411]-[0412]), while Fitzgerald teaches an SOI structure with a layered SOI composition, in particular SiGe on Si (Figure 1) for the specific purpose to enhance electron mobility (see "Background of the Invention"). *Motivation* to follow the suggestion by Yonehara et al and the teaching by Fitzgerald immediately derives from the improved electron mobility and consequent higher operational speed.

*On claims 8 and 9,* both Yonehara et al ([0411]-[412] and Fitzgerald ([0032] and Figures 4) teach the silicon layer to be formed in an SOI structure, i.e., inherently a structure in which the silicon crystal layer is separated by a silicon oxide layer, i.e., said semiconductor substrate is an SOI substrate wherein the crystal layer is an upper silicon crystal layer separated by a silicon dioxide layer (loc.cit.).

*On claim 10:* while Yonehara et al teach SIMOX as a method in the prior art for making an SOI substrate ([0006]) Applicant is reminded that the limitation of claim 10 fails to further limit the device and instead only further limits the method of making. Therefore, the further limitation defined by claim 10 fails to distinguish over the prior art.

*On claim 11:* similarly, while Yonehara et al teach bonding steps the limitation of claim 11 fails to further limit the device but instead only limits its method of making. Hence the further limitation fails to distinguish over the prior art.

4. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al as and APAA applied to claim 1 above, and further in view of Hurley (5,698,474).

*As detailed above, claim 1 is unpatentable over Yonehara et al in view of APAA, neither necessarily teaching the further limitation defined by claim 12.*

*However, it would have been obvious to include said further limitation in view of Hurley, who, in a patent on semiconductor wafer manufacturing for integrated circuits, hence analogous art, teaches exposing the entire backside as a flat, thinned and mirror polished for the specific purpose of creating a window suitable for inspection (see title, abstract and col. 5, lines 8-12). Motivation for the inclusion of the teaching by Hurley in this regard in the invention by Yonehara derives from the need to inspect the quality of the result of the manufacturing process.*

5. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al and APAA as applied to claim 1 above, and further in view of Steckl et al (5,759,908). As detailed above, claim 1 is unpatentable over Yonehara et al in view of

APAA. Neither necessarily teach the further limitation defined by claim 13. However, it would have been obvious to include SiC as a substrate material for an SOI in view of Steckl et al, who teach silicon carbide SOI structures (title, abstract) for the specific purpose of *inter alia* its higher breakdown voltage (see col. 1, l. 10-22). *Motivation* to replace the silicon substrate with the silicon carbide substrate derives immediately from said higher breakdown voltage.

6. **Claims 19-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara in view of APAA and Steckel et al (all as previously cited).

*On claim 19:* As pointed out under "Double Patenting", claim 19 is an essential copy of claim 13 through the latter's dependence upon claim 1 and hence the explanation of the rejection can be abbreviated as the explanations rejections of both claim 1 and of claim 13 are already on file (see said rejections overleaf). Said explanations are herewith included by reference in their entirety.

*On claim 20:* a maximum value of a thickness of the crystal layer 10 is defined by Yonehara to be 20  $\mu\text{m}$  (see [0150]), which does satisfy the claimed inequality for a required concentration of boron [B] (in atoms/cm<sup>3</sup>), said concentration being required to be in the interval  $10^{17} - 10^{20} \text{ cm}^{-3}$  (see [0149]), hence  $10^{20}$  being one of all required values, because  $\exp(0.21 \times 20) = \exp(4.2) \cong 66.7 \leq 4166 \leq 10^{20} / (2.2 \pm 0.2) \times 10^{16} \leq 10^{20} / (2.2 \pm 0.2) \times 10^{16}$ .

*On claim 21:* the crystal layer 10 is a silicon crystal layer ([0078]) formed by epitaxial growth ([0149]).

*On claim 22:* the crystal layer is a silicon-germanium alloy crystal layer ([0078]).

7. **Claim 23-27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al, APAA and Steckel et al as applied to claim 19 above, and further in view of Fitzgerald (US 2002/0123167 A1).

As detailed claim 2 is unpatentable over Yonehara et al in view of APAA. Neither necessarily teach the claimed layered structure of SiGe and Si. However, (a) there is a specific suggestion by Yonehara et al that a layered structure of SiGe on silicon could be used to generate stress in an SOI structure ([0411]-[0412]), while Fitzgerald teaches an SOI structure with a layered SOI composition, in particular SiGe on Si (Figure 1) for the specific purpose to enhance electron mobility (see "Background of the Invention").

*Motivation* to follow the suggestion by Yonehara et al and the teaching by Fitzgerald immediately derives from the improved electron mobility and consequent higher operational speed.

*On claims 24-25*, both Yonehara et al ([0411]-[412] and Fitzgerald ([0032] and Figures 4) teach the silicon layer to be formed in an SOI structure, i.e., inherently a structure in which the silicon crystal layer is separated by a silicon oxide layer, i.e., said semiconductor substrate is an SOI substrate wherein the crystal layer is an upper silicon crystal layer separated by a silicon dioxide layer (loc.cit.).

*On claim 26*: while Yonehara et al teach SIMOX as a method in the prior art for making an SOI substrate ([0006]) Applicant is reminded that the limitation of claim 26 fails to further limit the device and instead only further limits the method of making. Therefore, the further limitation defined by claim 10 fails to distinguish over the prior art.



Art Unit: 3663

On claim 27: similarly, while Yonehara et al teach bonding steps the limitation of claim 27 fails to further limit the device but instead only limits its method of making.

Hence the further limitation fails to distinguish over the prior art.

8. **Claim 28** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al as, APAA and Steckel et al applied to claim 19 above, and further in view of Hurley (5,698,474).

*As detailed above, claim 1 is unpatentable over Yonehara et al in view of APAA and Steckel et al, neither necessarily teaching the further limitation defined by claim 28.*

*However, it would have been obvious to include said further limitation in view of Hurley, who, in a patent on semiconductor wafer manufacturing for integrated circuits, hence analogous art, teaches exposing the entire backside as a flat, thinned and mirror polished for the specific purpose of creating a window suitable for inspection (see title, abstract and col. 5, lines 8-12). Motivation for the inclusion of the teaching by Hurley in this regard in the invention by Yonehara derives from the need to inspect the quality of the result of the manufacturing process.*

### ***Double Patenting***

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

9. Applicant is advised that should claim 13 be found allowable, **claim 19** will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### ***Response to Arguments***

Applicants' arguments filed 5/7/07 have been fully considered but they are not persuasive.

Applicants' traverse consists of two arguments:

- (a) an argument against the prima facie obviousness rejection;
- (b) an argument based on an allegation of unexpected results.

In support of argument (a) applicants allege that:

(a.1) "The Examiner is treating the claimed invention as having a single parameter, boron concentration" (page 9 of Remarks). However, this is not true: the rejection clearly takes into account a combination of values for boron concentration and thickness showing that the combination fulfills the semi-inequality as claimed (see pages 3-4 of the Final Office Action mailed 2/7/07. In the two-dimensional parameter space (plane) of thickness and boron concentration applicant claims a region defined by the claimed semi-inequality; while the rejection shows that the (rectangular) range in the same two-dimensional plane taught by Yonehara et al. as defined in paragraphs as

cited ([0149] and [0150]) substantially overlaps the range as claimed. Neither the grounds for rejection nor the case law, i.e., in re Peterson, as provided in the office action as cited are invalid because of the two-dimensional rather than one-dimensional character of the range. Applicants, through their claimed range, are on record that all two-dimensional points in said plane are good for the invention. Therefore, applicants' argument fails to persuade.

(a.2) Applicants further argue against the *prima facie* obviousness rejection by calculating a "chance" of a randomly selected boron concentration and substrate (sic) layer thickness (crystal layer thickness) from Yonehara et al. to meet the claimed semi-inequality. By presenting this argument, applicants engage in traversing not just the rejection but any conclusion of *prima facie* obviousness merely based on a finding of an overlapping range, because the same calculation can be performed in the case of a one-dimensional range. Claiming a single point would surely diminish the chance of finding the claimed invention in the prior art, but neither applicants nor the courts can be expected to believe that this diminished chance would cement the case in favor of granting a patent for a single point "range". Furthermore, applicants do not provide any explanation or detailed calculation in support of their quantitative statement, while a simple counterexample is already on record, one that on the basis of the numerical details can easily be checked or refuted, and which shows that for the thickness of just over 100 nm = 0.1  $\mu\text{m}$  the inequality is met for a subset of boron concentration values (see page 3 of the Final Office action mailed 2/7/07). Applicants neither traverse said

numerical details nor explain how to achieve their own results. Therefore, said argument (a) fails to persuade.

In support of argument (b) on "unexpected results", applicants argue first (page 11) based their rationale for the claimed upper limit for the boron concentration and that said rationale is absent in Yonehara et al. However, "unexpected results" and "different rationale" are entirely different concepts, and frankly, examiner sees no connection between the two. Second, applicants reiterate the allegation (page 12) that unexpected results are the basis for the claimed range. However, the Specification as a whole does not provide any evidence for this allegation, which, considering the two-dimensional but open-ended nature of the relation between boron concentration and thickness would have required the presentation of figures-of-merit in dependence of location in aforementioned two-dimensional plane, with solid experimental quantification including err bars. Such is absent from the Specification.

Therefore, said argument (b) also fails to persuade.

On the new claims: Applicants additionally draw attention to new claims 19-28 (see page 12 of Remarks), alleging claim 19 to introduce a new limitation on carbon concentration. However, said limitation on carbon concentration is identical to the further limitation defined by claim 13 while otherwise being identical to claim 1 upon which claim 13 depends. Therefore, claim 19 is a case of possible double patenting under 35 U.S.C. 101, and a warning to this effect has been issued overleaf. As for the merits, all claims stand rejected over the same prior art as applied to claims 1 and 4-14.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 3663

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM  
August 7, 2007

Primary Patent Examiner:

A handwritten signature in black ink, appearing to read 'J. Mondt', is written over a horizontal line.

Johannes Mondt (TC 3600, Art Unit: 3663)